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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/114,203	07/13/1998	ATSUSHI MIYANISHI	030682-066	8932

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[REDACTED] EXAMINER

BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/114,203

Applicant(s)

Miyanishi et al.

Examiner

B. William Baumeister

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on Mar 8, 2002

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) Claim(s) 2-4, 6-11, and 13-24 is/are pending in the application.

4a) Of the above, claim(s) 2-4 and 6-11 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 13-24 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on Jul 13, 1998 is/are objected to by the Examiner.

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) All b) Some* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) Notice of References Cited (PTO-892)

18) Interview Summary (PTO-413) Paper No(s). _____

16) Notice of Draftsperson's Patent Drawing Review (PTO-948)

19) Notice of Informal Patent Application (PTO-152)

17) Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

20) Other: _____

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DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Species III in Paper No. 26 is acknowledged.

Drawings

2. As was mentioned in the restriction requirement of paper # 26, Figures 16, 19 and 22 appear to illustrate only that which is old. Accordingly, Applicant should so designate these figures by a legend such as --Prior Art-- (See MPEP § 608.02(g)) or alternatively provide sufficient explanations as to why these are not depictions of conventional circuit diagrams.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13, 17-19, 23 and 24 rejected under 35 U.S.C. 103(a) as obvious over Shou et al. '859 in view of NSC WO '898.

- a. Shou depicts inverter circuits having various active regions including PL1 and NL1. See e.g., PL1 wherein a recessed region (strangulation region S1) is disposed between two

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ordinary regions. The left portion of the ordinary region has a first gate electrode G disposed between S/D regions having contacts C1 and C3, respectively. The strangulation region has a second gate electrode G. Both of these gates have upper ends which are formed in a line.

While the reference unequivocally depicts the two gates terminating at a common line, the reference does not expressly depict this common line being at a point that is beyond the edge of the active region PL1 (i.e., the reference does not expressly depict the presence of end caps). Nonetheless, one skilled in the art would understand that the gate of the ordinary region must necessarily extend at least some distance onto the surrounding oxide region (i.e., that the end caps must necessarily be present on both gates); otherwise the source/drain regions of the ordinary region would be inclined to short and the transistor would not operate as intended. Thus, Shou inherently discloses the presence of the end caps.

b. Alternatively, even assuming *arguendo* that Shou must be interpreted so narrowly as not expressly teaching the presence of the end cap on the ordinary region, the claims would be obvious since its presence is implied. Further, NSC discloses that poly end cap rounding is a conventional problem wherein an end cap does not sufficiently extend onto the surrounding oxide, resulting in undesirable leakage currents. The reference further discloses that it was conventional to avoid this problem by increasing the distance between the poly end cap and the parallel edge of the field oxide (i.e., the margin) (page 1, Discussion of Prior Art and particularly lines 30-33). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the gate in the ordinary region of the Shou reference must--or at least very preferably should-

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-also possess an end cap margin for the purpose of preventing the undesired current leakage, as taught by NSC.

c. Shou also depicts the strangulation region as having a semicircular shape as opposed to being formed by first, second and third edges at right angles. NSC teaches a FOX protrusion/active area recess with sides formed at right angles (see e.g., FIG 1A). It would have been obvious to one of ordinary skill in the art at the time of the invention to form the recessed portion of Shou with straight sides having right angles--at least to the extent afforded by then-existing processing techniques--as taught by NSC for conventional business reasons such as for simplifying the mask design and manufacturing process.

5. Claims 14-16 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shou '859/NSC '898 as applied to the claims above, and further in view of Jassowski et al. 389.

a. As was stated above, Shou teaches either alone or in combination with NSC '898 active regions having gates extending from ordinary regions and recessed regions wherein the gate margin of the recessed region extends so that its end is in line with that of the ordinary gate's end. NSC '898 depicts (see FIGS 1A-1C) gate end caps that extend onto a recessed portion that has first and second edges extending perpendicular to the third edge thereby forming the recess. NSC further teaches that it was conventionally known that the gate margin may be increased in this situation to prevent S/D shorting or punchthrough. Neither Shou nor NSC teaches that the first edge may be longer than the second edge, as required by claims 14 and 20.

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b. Jassowski '389 depicts (See Fig 2 as labeled by the Examiner) at least one active region having an ordinary region from which gate 3 extends and having a first edge E1; a second region having a second edge E2 that is shorter than E1; and a depressed region having an edge E3 from which gate 4 extends. Both of these gates 3 and 4 have endcap margins. It would have been obvious to one skilled in the art at the time of the invention to provide an active region having a first edge that is longer than the second edge, as taught by Jassowski depending only upon the specific application for which the active region is to be employed.

c. Claims 14 and 20 further require that the endcap margin length of the recessed gate be longer than the second length. While the margin of gate 4 is not longer, the claims nonetheless would have been obvious for the following reasons:

i. Jassowski teaches a lower boundary limit of having the second gate length shorter than the second edge while Shou teaches the upper boundary limit wherein the second gate length is not only longer than the second edge, it also extends to the same line as that of the first gate length. Coupling these two boundary points with the teachings of NSC--that either (1) the length of a recessed gate's margin may be increased or (2) that the lateral spacing to the edge of the field oxide may be increased in order to ensure that no shorting occurs, renders it obvious to one of ordinary skill in the art at the time of the invention that the length of the recessed gate margin could alternatively be formed of any length intermediate between these lower and upper boundary limits, depending only upon the specific application intended for the active region as this dictates various conventional details such as the channel width and length, which in turn, dictates

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the length and spacing requirements for the three edges of the recessed portion and the layout constraints for the circuit cell.

ii. This position is further supported by other teachings of Jassowski.

Specifically, gate 1 is also formed on another recessed portion. This gate is disposed so closely to the edge E5 that the gate length is set at a length of E5 + the length of the margin of gate 2. Note that E5 is less than E1. This provides support for the position that in those situations wherein a recessed gate is formed very close to an active edge (be it in the middle of an active region as set forth in claims 15 and 21 or at a corner region as depicted in the specific embodiment of Jassowski), it would have been obvious to one skilled in the art at the time of the invention to extend the gate to the same length that is set for the margin of the non-recessed region for the purpose of preventing shorting in case of misalignment or rounding, as taught by Jassowski and NSC.

d. Again, the foregoing analysis sets forth the boundary conditions for the recessed gate's margin length and various reasons for altering this length anywhere in between these two points. As such, these reasons also render claims 16 and 22 obvious because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. In the present case, the general conditions and the working ranges have been taught by the combination of the prior art references, and setting the gate length as set forth by these claims does not provide any unexpected results.

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Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Tamura '811 teaches ordinary region 15 having a first length; transistor 111 having a portion adjacent contact 145 with a second length less than that of the first length; and a recessed portion of transistor 111 and recessed transistor 112; and gates with endcaps being formed on the recessed and ordinary regions.

b. Bergemont et al. '754 teaches that steps must be taken to account for misalignment of poly lines on field oxides adjacent active regions.

c. Bergemont 478 teaches poly lines on recessed portions of field oxides.

INFORMATION ON HOW TO CONTACT THE USPTO

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister**, at (703) 306-9165. The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.



B. William Baumeister

Patent Examiner, Art Unit 2815

March 17, 2002